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Serial No. 09/943,196

Filing Date: August 30, 2001

Examiner: Lynette T. Umez-Eronini

n re patent application of: Charles E. May

Group Art Unit: 1765

For: Arrangement and Method for Fabricating a Semiconductor Wafer

TO THE COMMISSIONER OF PATENTS AND TRADEMARKS:

Sir:

This is a Request for Continued Examination under 37 C.F.R. § 1.114(a) of application number 09/943,196, filed on August 30, 2001, entitled Arrangement and Method for Fabricating a Semiconductor Wafer. Transmitted herewith is a Submission in Response to the Final Office Action dated March 6, 2003 as per 37 C.F.R. § 1.114(c). The Submission includes a Response to Office Action, a Rule 1.131 Declaration of Charles E. May, and Exhibit A to the Rule 1.131 Declaration of Charles E. May

The Commissioner is hereby authorized to charge the fee set forth in 37 CFR §1.17(e) (i.e. \$750.00) for submission of a Request for Continued Examination to Deposit Account No. 12-2252. Two copies of this sheet are enclosed.

Harold C. Moore

Name of authorized person

Signature of authorized person Attorney for Applicant

Please address correspondence to:

Sandeep Jaggi c/o Mark Salvatore LSI Logic Corporation Mail Stop D-106 1551 McCarthy Boulevard Milpitas, California 95035

Please provide any further extensions of time which may be necessary and charge any fee which may be due to Deposit Account No. 12-2252, but not to include any payment of issue fees.

August 6, 2003 Maginot, Moore & Bowman, LLP Bank One Tower/Center 111 Monument Circle, Suite 3000 Indianapolis, Indiana 46204-5115 (317) 638-2922

Harold C. Moore Attorney for Applicants Registration No. 37,892

Respectfully submitted,

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